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(54) Process for manufacturing electronic devices comprising high voltage mos transistors, and electronic device thus obtained

(57) For manufacturing an HV MOS transistor (80) having a low multiplication coefficient and a high threshold, a non-implanted area (6) of the substrate is used. This area thus has the same conductivity type and the same doping level as the substrate. The transistor is obtained by forming, over the non-implanted substrate area, a first gate region (43a) of semiconductor material having the same doping type as the non-implanted substrate area; and forming, inside the non-implanted substrate area, first source and drain regions (64a) of a second conductivity type, arranged at the sides of the first gate region (43a). At the same time, also a dual-gate HV MOS transistor (81) is formed, the source and drain regions (64b) of which are housed in a tub (13) formed in the substrate (2) and having the first conductivity type, but a higher concentration than the non-implanted substrate area. It is moreover possible to form a nonvolatile memory cell (82) simultaneously in a second tub (14) of the substrate (2) of semiconductor material.

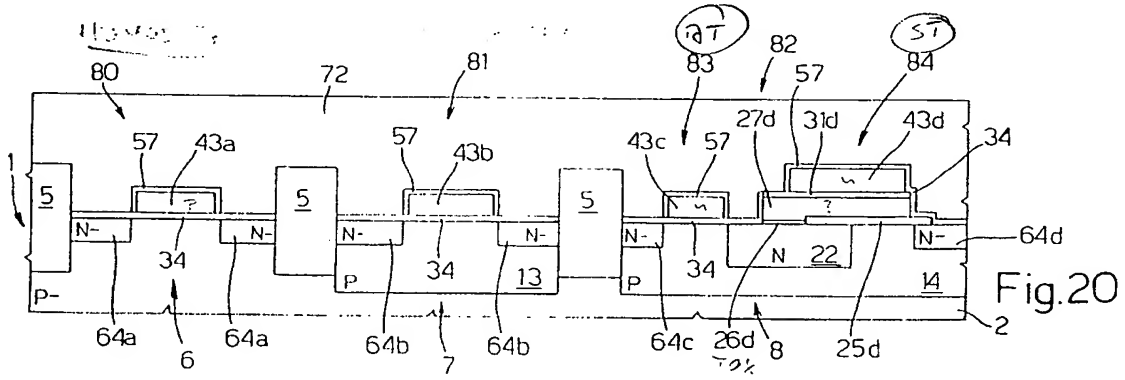

Fig.20

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Description

[0001] The present invention regards a process for manufacturing electronic devices comprising high voltage MOS transistors, and an electronic device thus obtained.

[0002] Many electronic devices currently present on the market use both NMOS and PMOS high voltage transistors (hereinafter referred to as HV transistors) of the dual-gate type (i.e., having the gate region doped with doping ionic species of the same type used for the source and drain regions) and of the drain-extension type. In these manufacturing processes, in order to achieve lengths of the channels of the HV transistors of less than 0.5 μm it is necessary to appropriately increase the doping of the substrate so as to prevent undesired effects, such as punchthrough, i.e., the undesired electrical connection between two regions having different potentials. For this reason, the region designed to house these transistors is enriched with doping ions that may confer on the region the same conductivity type as the substrate, forming a well (or tub) that has a doping level greater than the substrate.

[0003] In many devices it is, however, also indispensable to have HV transistors with a low multiplication coefficient (i.e., with a low ratio between the current flowing in the drain region and the current flowing in the substrate) and with a low body effect (i.e., a reduced increase in the threshold voltage of the transistor when the substrate biasing voltage increases), which features require a low doping of the substrate.

[0004] A commonly adopted solution to this problem is that of suitably shaping the masks so as to form so-called "NO-TUB" HV transistors formed directly in the substrate, instead of in the well or tub.

[0005] Since these transistors have a low multiplication coefficient but also a low threshold voltage, they can be used only with appropriate circuit solutions to prevent unacceptable parasitic currents. On the other hand, such solutions lead to an undesired complication of the circuitry associated to the HV transistors. The aim of the present invention is therefore to provide a new process for manufacturing electronic devices comprising HV transistors with a low multiplication coefficient, a low body effect, and a high threshold.

[0006] According to the present invention, a process for manufacturing electronic devices comprising HV transistors is provided, as defined in Claim 1. The invention moreover refers to an electronic device as defined in Claim 7.

[0007] For a better understanding of the present invention, a preferred embodiment thereof is now described, purely as a non-limiting example, with reference to the attached drawings in which:

- Figure 1 shows a cross-section through a wafer in an initial step of the manufacturing process according to the present invention;
- Figure 2 presents a top view of the wafer of Figure 1;
- Figures 3-9 show cross-sections similar to that of Figure 1 during successive manufacturing steps;
- Figure 10 presents a top view of the wafer of Figure 9;
- Figures 11-13 show cross-sections similar to that of Figure 9 during successive manufacturing steps;
- Figure 14 presents a top view of the wafer of Figure 13;
- Figure 15 shows a cross-section similar to that of Figure 11 in a subsequent manufacturing step;
- Figure 16 presents a top view of the wafer of Figure 15;
- Figure 17 shows a cross-section similar to that of Figure 15 in a subsequent manufacturing step;
- Figure 18 presents a top view of the wafer of Figure 17; and
- Figures 19-20 show cross-sections similar to that of Figure 17 in successive manufacturing steps.

[0008] The following description refers to an embodiment of HV NMOS transistors of a traditional type (and hence with a high multiplication coefficient), HV NMOS transistors with a low multiplication coefficient and a high threshold, and EEPROM memory cells including a selection transistor and a memory transistor.

[0009] In Figure 1, a wafer 1 comprising a substrate 2 of P-type monocrystalline silicon has undergone the steps of definition of the active areas. In detail, in a per se known manner, thick oxide regions (field oxide regions 5) have already been formed in the substrate 2, these regions delimiting between them active areas of the substrate that are to house various components of the device to be formed. In particular, Figure 1 shows three such active areas: a first active area 6 for housing first HV transistors having a low multiplication coefficient and a high threshold (hereinafter also referred to as NO-TUB HV transistors), a second active area 7 for housing second HV transistors having a high multiplication coefficient, and an active matrix area 8 for housing EEPROM memory cells. Further active areas (not shown in the drawings) are generally provided for forming LV NMOS and PMOS transistors or HV PMOS transistors.

[0010] In detail and in a per se known manner, the active matrix area 8 defines a grid, of which Figure 2 shows in full only the part regarding a cell, indicated by 9, having basically the shape of a T rotated through 90°.

[0011] A sacrificial oxide layer 10 extends on surface 3 of substrate 2.

[0012] Subsequently, as shown in Figure 3, an HV P-well resist mask 11 is formed which covers the entire surface of the wafer 1, except for the second active area 7 and the active matrix area 8, and P-type doping species are implanted, as schematically represented by arrows 12. The implant gives rise to an HV P-type tub 13 in the first active area 7 and to a P-matrix tub 14 in the active area 8. The HV P-type tub 13 and P-matrix tub 14 thus have the same conductivity type as the sub-

strate 2, but a higher doping concentration. Instead, the first active area 6 is not implanted to enable formation of the NO-TUB HV transistors.

[0013] After removing the HV P-well mask 11, a capacitor mask 20 is formed which covers the entire surface of the wafer 1, except for strips perpendicular to the plane of the drawing. Next, N-type doping species (e.g., phosphorus) are implanted, as represented schematically in Figure 4 by arrows 21. N-type continuity regions 22 are then formed inside the P-matrix tub 14 providing electrical continuity between each selection transistor and the respective memory transistor of each cell.

[0014] After removing the capacitor mask 20, the wafer 1 is annealed, the sacrificial layer 10 is removed, and matrix oxidation is carried out, so as to form a matrix oxide layer 25 over the surfaces of all the active areas 6, 7, 8, as shown in Figure 5. Next, using a matrix oxide mask 24 which covers only the wafer 1 above the P-matrix tub 14, where the gate regions of the memory transistors are to be formed, the matrix-oxide layer 25 is removed where it is uncovered to form a matrix oxide region 25d in the P-matrix region 14 partially covering the continuity region 22 (Figure 6).

[0015] After removing the matrix oxide region 24, the wafer 1 is again oxidized to form a tunnel oxide layer 26 over the entire surface 3 of the wafer 1, where the latter is exposed, and the thickness of the matrix oxide region 25d increases. In this way, the structure of Figure 7 is obtained.

[0016] A first polycrystralline silicon layer (polyl layer 27) is then deposited and appropriately doped. Subsequently, an interpoly dielectric layer 31 is formed, for example comprising a triple ONO (silicon oxide - silicon nitride - silicon oxide) layer, as shown in figure 8.

[0017] A floating gate mask 30 is then formed, as shown in Figures 9 and 10. Next, the dielectric layer 31, the polyl layer 27, and the tunnel oxide layer 26 are etched to form an interpoly dielectric region 31d, a floating gate region 27d, and a tunnel region 26d, which are aligned with respect to each other.

[0018] After removing the floating gate mask 30, an HV oxidation step is carried out, thus forming an HV gate oxide layer 34 over the entire free surface of the wafer 1 (Figure 11). Portions of oxide 34 are formed also at the sides of the floating gate region 27d of the memory transistor, as illustrated in Figure 11.

[0019] A second polycrystalline silicon layer (poly2 layer 43, not doped) is then deposited, as shown in Figure 12. A dual-gate doping mask 44 is then formed and covers the active area 6, as shown in Figures 13 and 14, and then N-type doping ionic species are implanted, as represented schematically by arrows 47 in Figure 13. In this way, the portions of the poly2 layer 43 over the HV P tubs 13 and P-matrix tubs 14 undergo N-type doping.

[0020] Next, using a selective doping mask 48, which covers the HV P tubs 13 and P-matrix tubs 14, P-type doping ionic species, for example boron, are implanted, as represented schematically by arrows 49 in Figure 15. In this way, the portion of the poly2 layer 43 which extends over the active areas 6 and is to form gate regions of the NO-TUB HV transistors undergoes P-type doping so as to present the same conductivity type as the substrate 2. Thereby, the structure shown in cross-section in Figure 15 and in top view in Figure 16 is obtained.

[0021] Next, using an HV gate mask 56, the poly2 layer 43 is selectively removed to form a gate region 43a, which is P-type doped, of the NO-TUB HV transistor, a gate region 43b, which is N-type doped, of the TUB HV transistor, a gate region 43c of the selection transistor of the memory cell, and a control gate region 43d of the memory transistor.

[0022] Next, a re-oxidation step is carried out, thus forming an oxide layer 57 over the entire free surface of the wafer 1, in particular at the sides of the gate regions 43a and 43b of the NO-TUB HV transistor and of the TUB HV transistor, as illustrated in Figure 19.

[0023] Subsequently, N-type doping ionic species are implanted, as represented schematically by arrows 63 in Figure 19. In the active area 6 and in the HV P tub 13 at the two sides of the HV gate region 43a of the NO-TUB HV transistor and of the HV gate region 43b of the TUB HV transistor, N-type source and drain regions 64a, 64b are formed.

[0024] Thus, the source and drain regions 64a of the NO-TUB HV transistor are doped in an opposite way with respect to their HV gate region 43a, whereas the source and drain regions 64b of the TUB HV transistor are doped in the same way as their HV gate region 43b. At the same time, in the P-matrix tub 14 the following regions are formed: a drain region 64c of the selection transistor, on one side and self-aligned with respect to the gate region 43c of the selection transistor; and a source region 64d of the memory transistor, on the side of the latter not facing the selection transistor, aligned with the gate region 43d of the memory transistor. In addition, an implant is carried out also on the area arranged between the selection transistor and the memory transistor; however, this implant is generally performed within the continuity regions 22, which are more doped, and hence is not visible (for this reason, the corresponding area has been represented by dashed lines in Figure 19). In the event of misalignments, however, this implant guarantees electrical continuity.

[0025] After a protective dielectric layer 72 has been formed, the final structure of Figure 20 is obtained, showing: a NO-TUB HV NMOS transistor 80 with P-type doped gate region 43a, a TUB HV NMOS transistor 81 with N-type doped gate region 43b, and hence of a dual-gate type, and an EEPROM cell 82 including a selection transistor 83 and a memory transistor 84. Final steps are the carried out, including forming the contacts and the electrical interconnection lines, depositing a passivation layer, etc.

[0026] The method described thus enables TUB HV transistors and NO-TUB HV transistors to be formed at

the same time, as well as memory cells having very different characteristics, optimizing the number of steps required.

[0027] In particular, the fact that the gate regions 43a of the NO-TUB HV transistors have the same conductivity type as the substrate 2 ensures a high work function (i.e., a high potential difference automatically present between materials because of the physical characteristics of the materials), and hence a high threshold voltage. Since the source and drain regions 64a are formed directly in the substrate 2, where a more doped tub is not present and the substrate 2 is not very doped, the NO-TUB HV transistors have a low multiplication coefficient and low body effect.

[0028] In this way, using a dual-gate process, it is also possible to obtain high threshold HV transistors, so avoiding the complex circuit solutions necessary for their use in prior art processes.

[0029] Finally, it is clear that numerous modifications and variations may be made to the method and device described and illustrated herein, all of which falling within the scope of the invention, as defined in the attached claims. For example, it is possible to form NO-TUB HV PMOS transistors, which will consequently have an N-type doped gate region, like the substrate, and P-type doped source and drain regions. Furthermore, the order of the steps for selectively doping the gate regions 43a, 43b and the control gate region 43d can be reversed, and these regions can be doped after they have been shaped, instead of before as has been described herein, possibly adjusting the implant dose of the source and drain regions 64a of the NO-TUB HV transistors.

Claims

1. A process for manufacturing electronic devices comprising a first high voltage MOS type transistor (80), comprising the steps of:

   - providing a substrate (2) of semiconductor material with a first area (6) having a first conductivity type and a first doping level;
   - forming a first gate region (43a) of semiconductor material of said first transistor (80) on said first area (6) of said substrate (2);
   - forming, in said first area (6) of said substrate (2), first source and drain regions (64a) of a second conductivity type, at the sides of said gate regions (43a);

   characterized in that it further comprises the step of doping said first gate region (43a) with doping species determining said first conductivity type.

2. The manufacturing process according to Claim 1, characterized in that it further comprises the step of forming a second high voltage MOS transistor (81) in a second area (7) of said substrate (2), and in that said step of forming said second high voltage transistor comprises the steps of:

   - forming, in said second area (7) of said substrate (2), a first tub (13) having said first conductivity type and a doping level higher than said first area (6) of said substrate (2);
   - forming a second gate region (43b) having said second conductivity type over said first tub (13); and
   - forming, in said first tub (13), second source and drain regions (64b) of said second conductivity type, laterally to said second gate region (43b).

3. The manufacturing process according to Claim 2, characterized in that said steps of forming first source and drain regions (64a) and forming second source and drain regions (64b) are performed simultaneously.

4. The manufacturing process according to Claim 2 or Claim 3, characterized in that said steps of forming said first gate region (43a) of said first transistor and of forming said second gate region (43b) of said second high voltage transistor are performed simultaneously.

5. The manufacturing process according to any of Claims 2-4, characterized in that it comprises the step of forming a nonvolatile memory cell (82) in a third area (8) of said substrate (2) of semiconductor material, and in that said step of forming said nonvolatile memory cell (82) comprises the steps of:

   - forming, in said third area (8) of said substrate (2), a second tub (14) having said first conductivity type and a doping level higher than said first area (6) of said substrate (2);
   - forming a floating gate region (27d) of said nonvolatile memory cell (82) over said second tub (14);
   - forming a control gate region (43d) of said second conductivity type, over said floating gate region (27d); and
   - forming, in said second tub (14), third source and drain regions (64d) of said second conductivity type, at the sides of said floating gate region (27d).

6. The manufacturing process according to Claim 5, characterized in that said steps of forming a first gate region (43a), a second gate region (43b), and a control gate region (43c, 43d) comprise a single step of depositing a semiconductor material layer (43), a single step of shaping, a first step of simultaneously doping said second gate region (43b) and

said control gate region (43c, 43d), and a second, separate, step of doping said first gate region (43a).

7. The manufacturing process according to Claim 5 or 6, characterized in that said step of forming third source and drain regions (64d) is performed simultaneously with said steps of forming said first source and drain regions (64a) and said second source and gate regions (64b).

8. The manufacturing process according to any of Claims 5-7, characterized in that said step of forming a nonvolatile memory cell (82) comprises the step of forming an EEPROM cell (82).

9. The manufacturing process according to any of the foregoing claims, characterized in that said first conductivity type is P-type and said second conductivity type is N-type.

10. An electronic device comprising:

- a substrate (2) of semiconductor material having a first area (6) with a first conductivity type and a first doping level; and
- a first high voltage MOS transistor (80), said first transistor comprising a first gate region (43a) of semiconductor material over said first area (6) of said substrate (2); first source and drain regions (64a) of a second conductivity type, housed in said first area (6) of said substrate (2), at the sides of said gate regions (43a); characterized in that said first gate region (43a) has a first conductivity type.

11. The electronic device according to Claim 10, characterized in that said substrate further comprises a first tub (13) having said first conductivity type and a doping level higher than that first area (6) of said substrate (2); and in that it further comprises a second high voltage MOS transistor (81), said second transistor (81) comprising a second gate region (43b) having said second conductivity type and being arranged over said first tub (13), and second source and drain regions (64b) of said second conductivity type, housed in said first tub (13) at the sides of said second gate region (43b).

12. The electronic device according to Claim 11, characterized in that said substrate further comprises a second tub (14) having said first conductivity type and a doping level higher than said first area (6) of said substrate (2); and in that it further comprises a nonvolatile memory cell (82) including a floating gate region (27d) over said second tub (14); a control gate region (43d) of said second conductivity type, over said floating gate region (27d); and third source and drain regions (64d) of said second conductivity type, housed in said second tub (14) at the sides of said floating gate region (27d).

13. The electronic device according to Claim 12, characterized in that said nonvolatile memory cell (82) is an EEPROM cell.

14. The electronic device according to any of Claims 11-13, characterized in that said first conductivity type is P-type, and said second conductivity type is N-type.

Fig.1

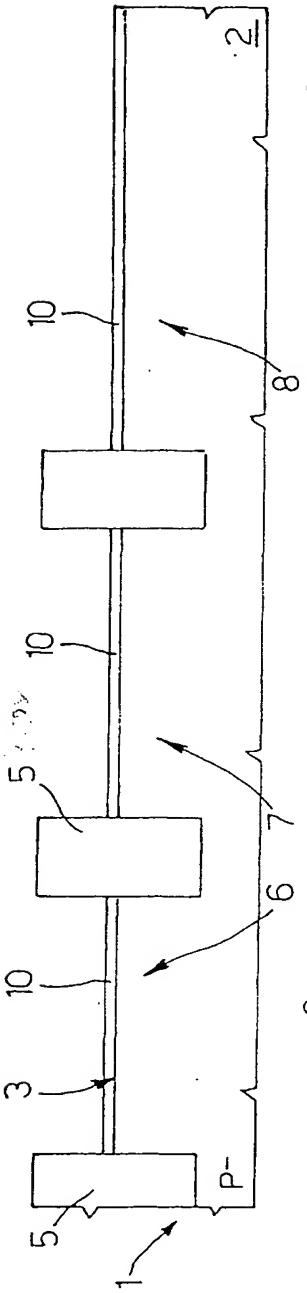

Fig.2

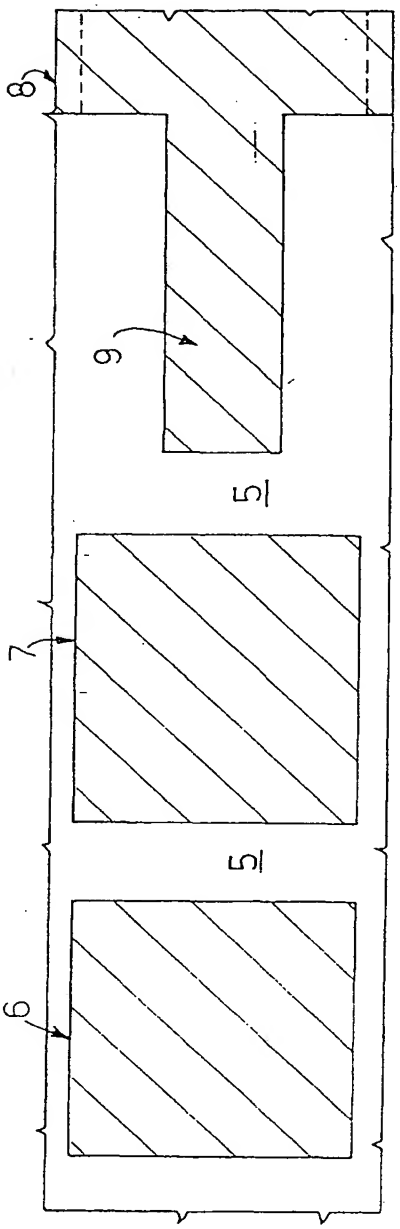

Fig.3

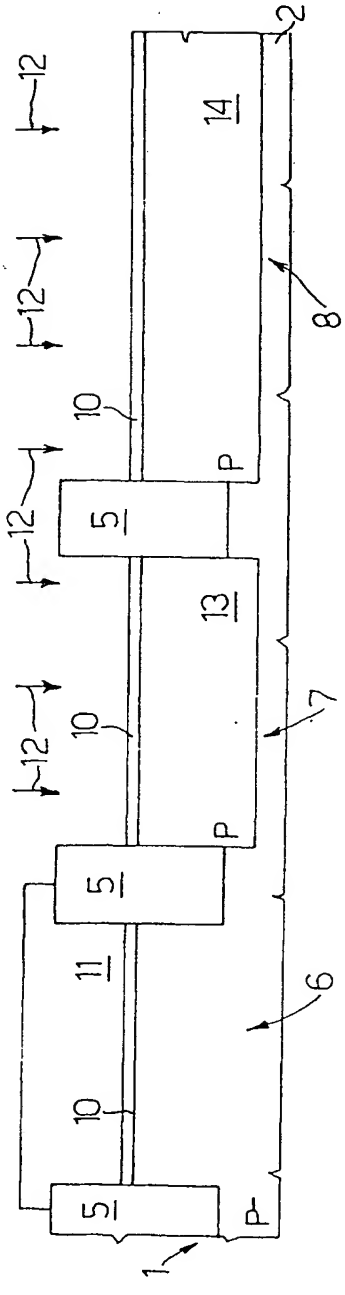

Fig.4

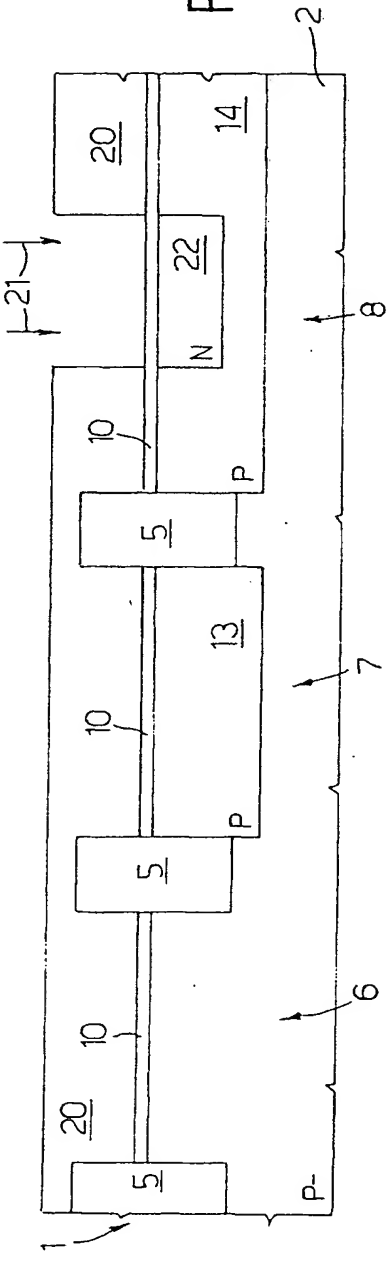

Fig.5

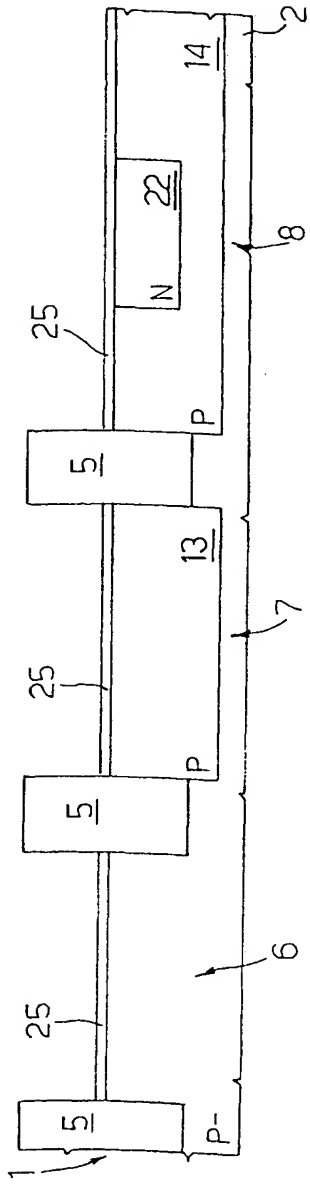

Fig.6

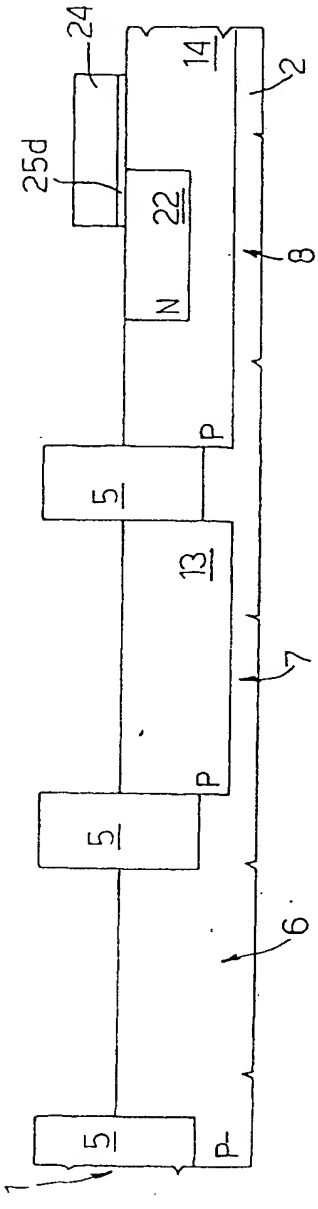

Fig.7

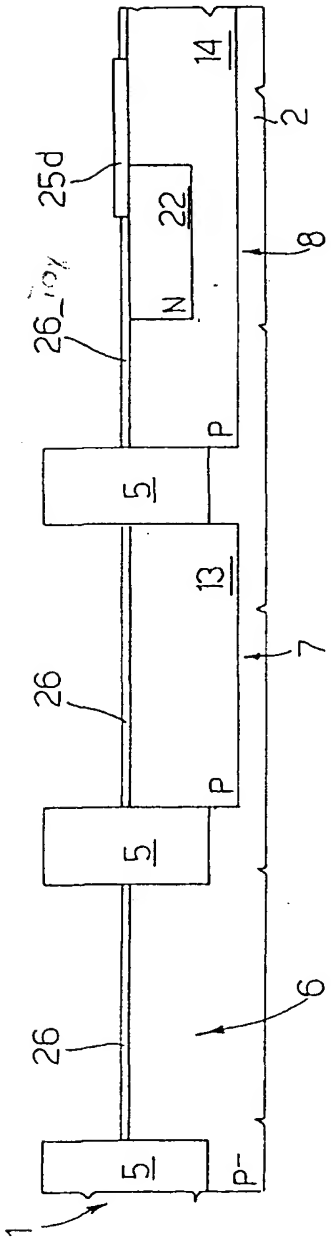
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Fig.8

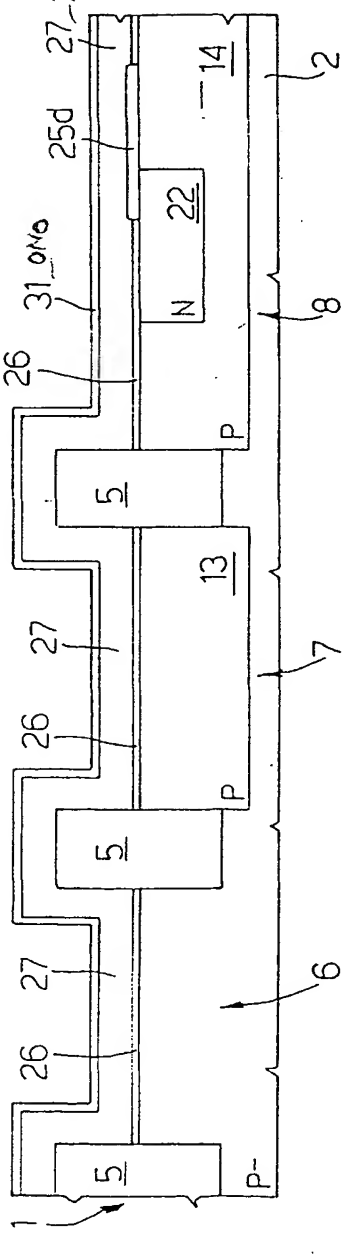
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Fig.9

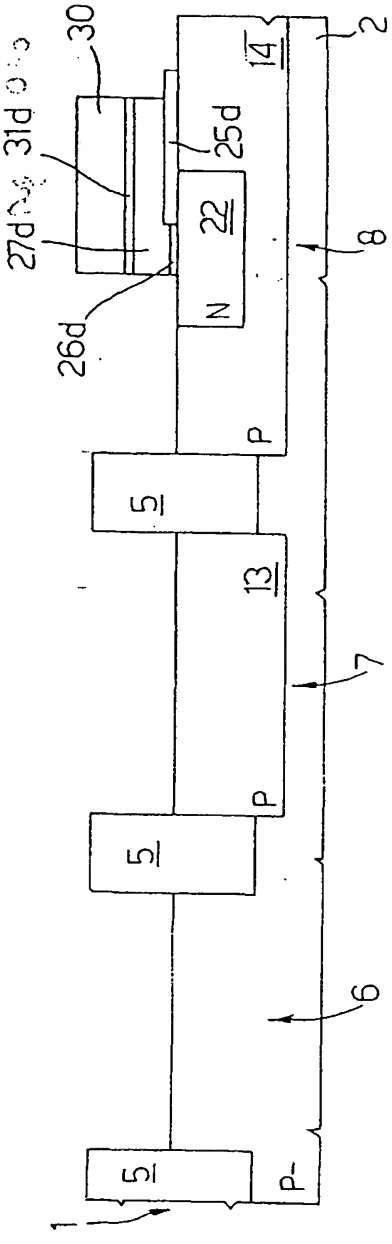

Fig.10

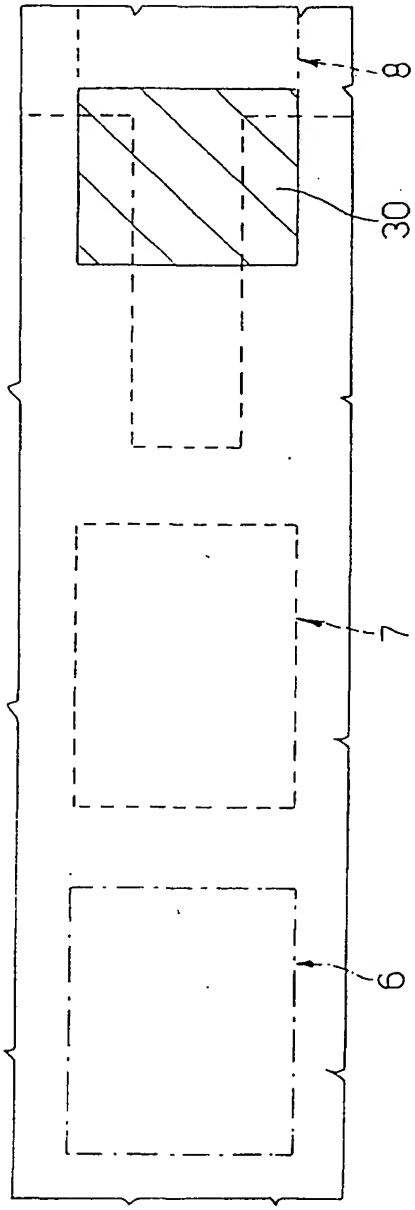

Fig.11

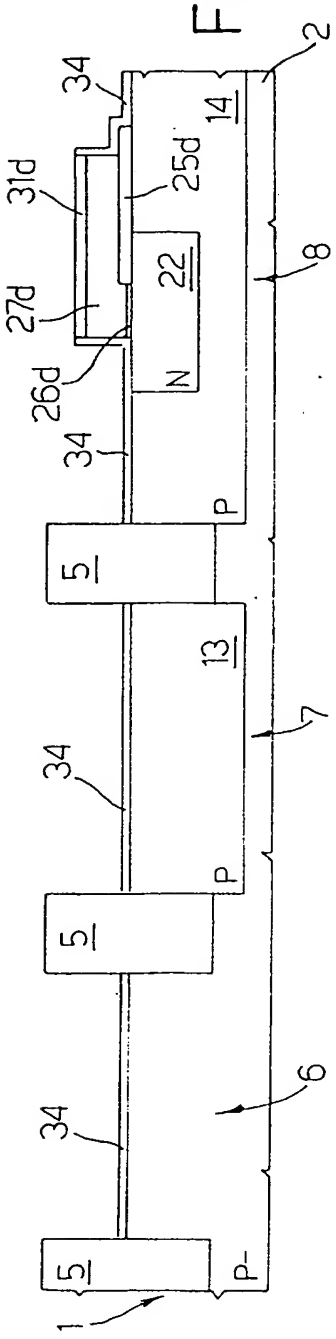
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Fig.12

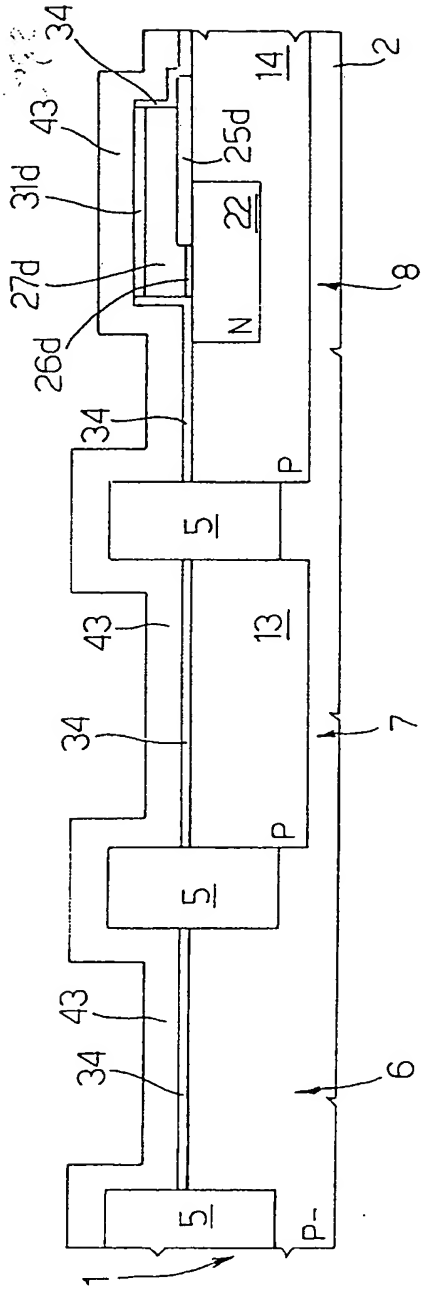
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Fig.13

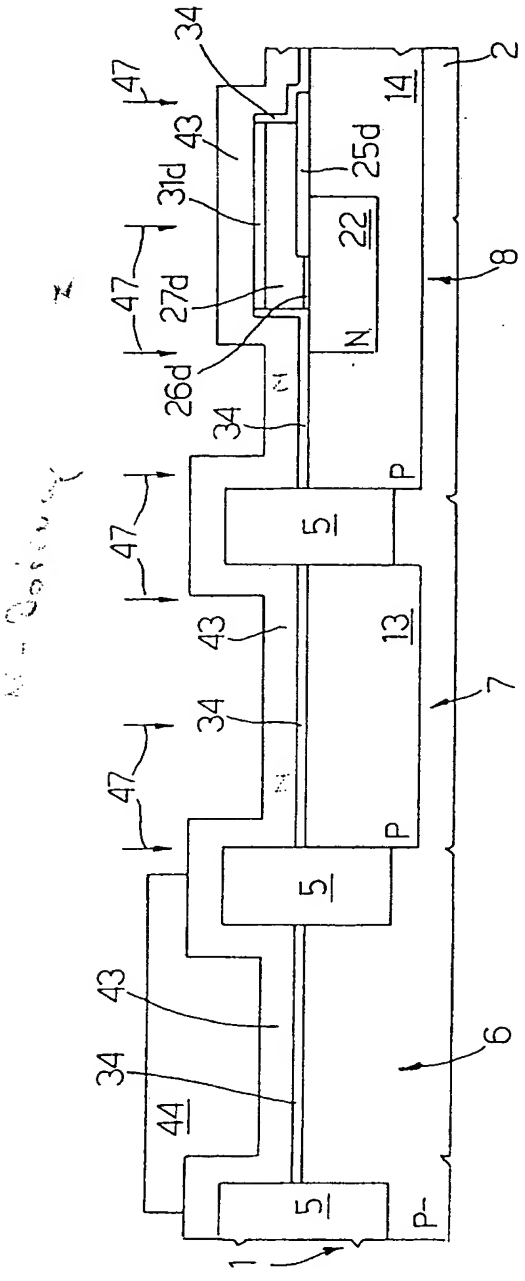
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Fig.14

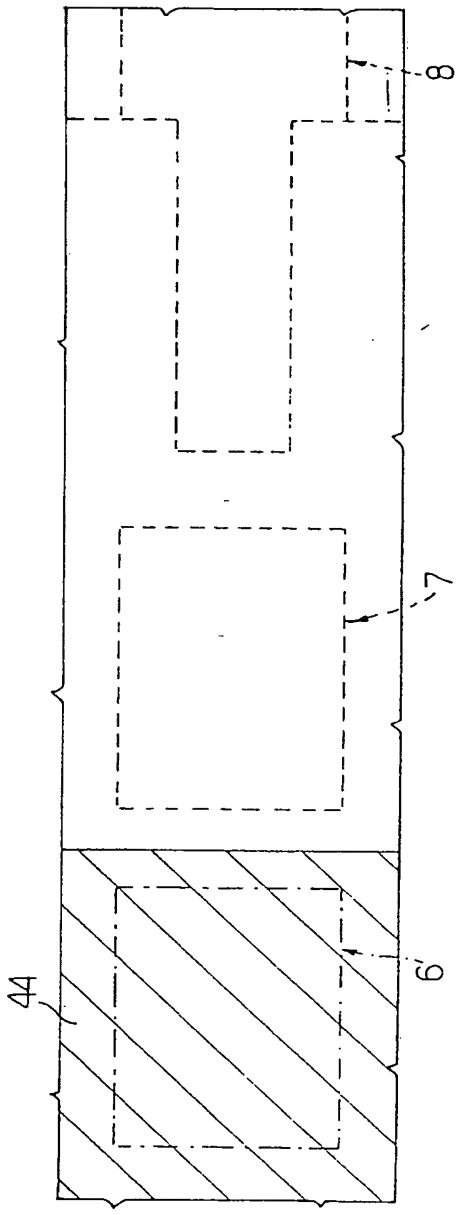
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Fig.15

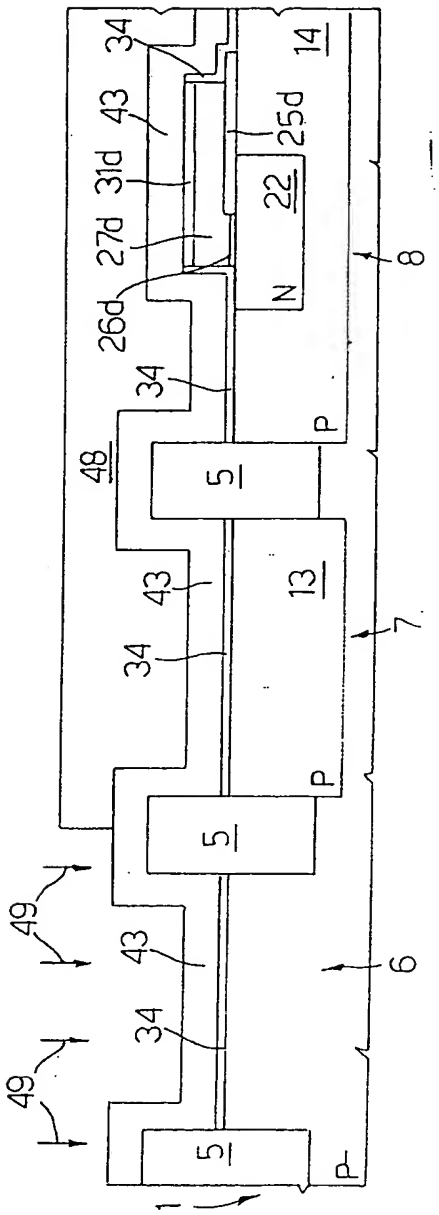
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Fig.16

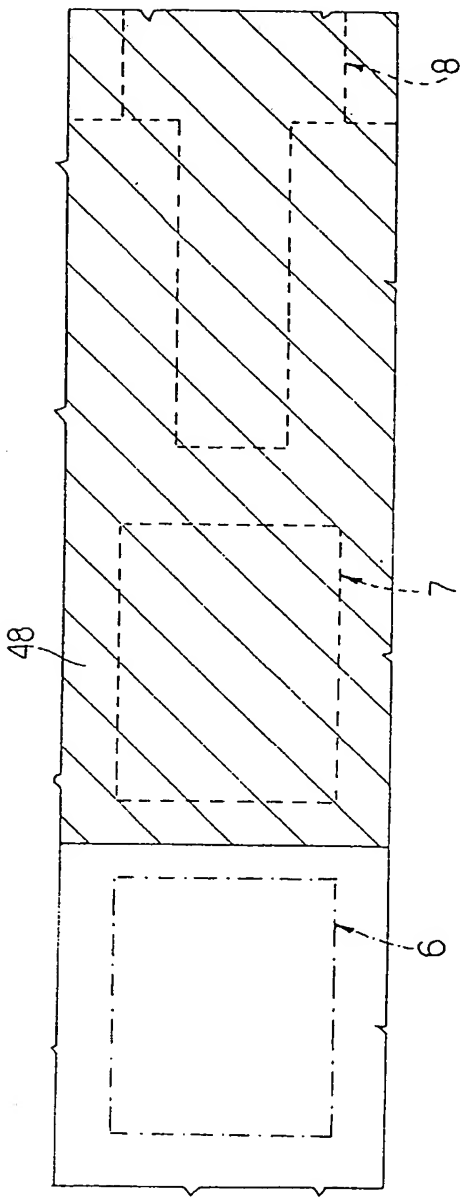
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Fig.17

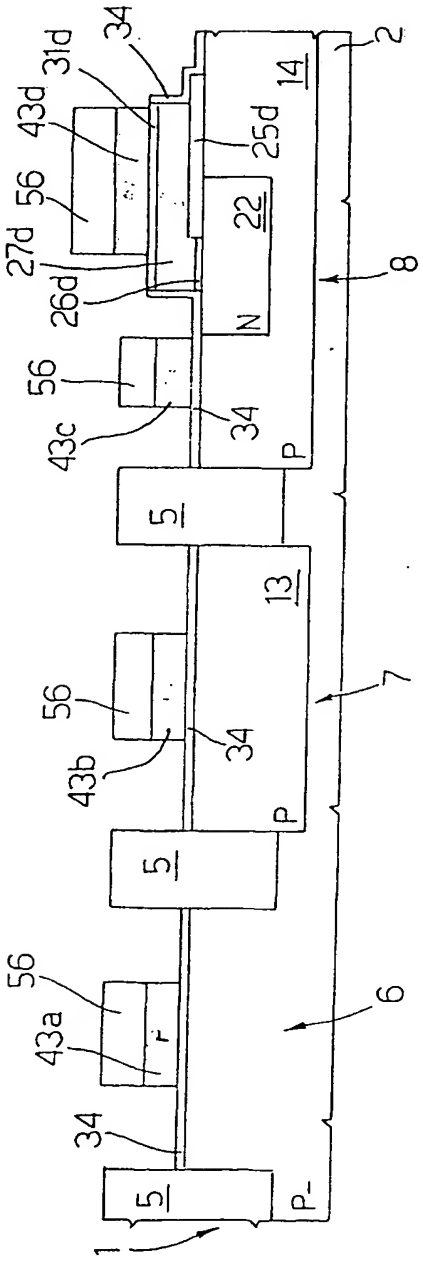
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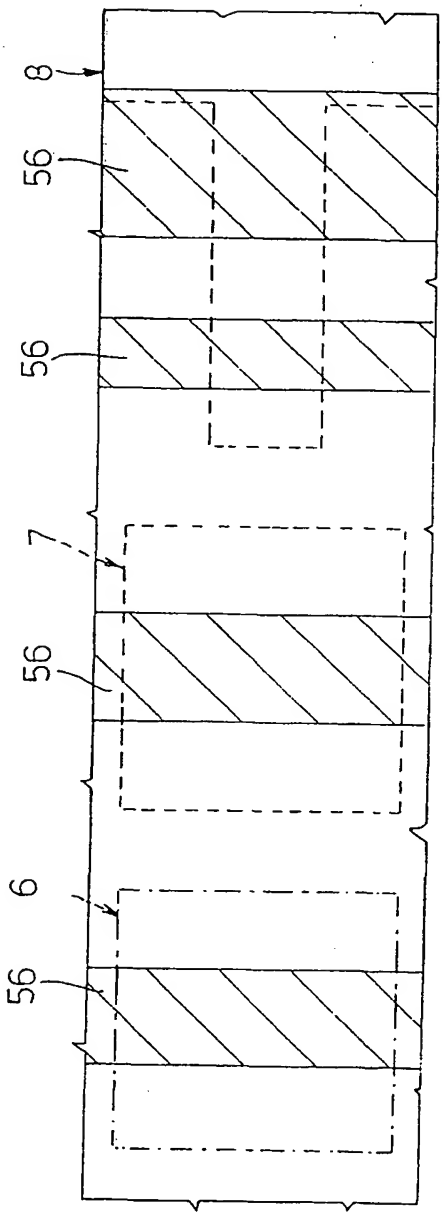
Fig.18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56

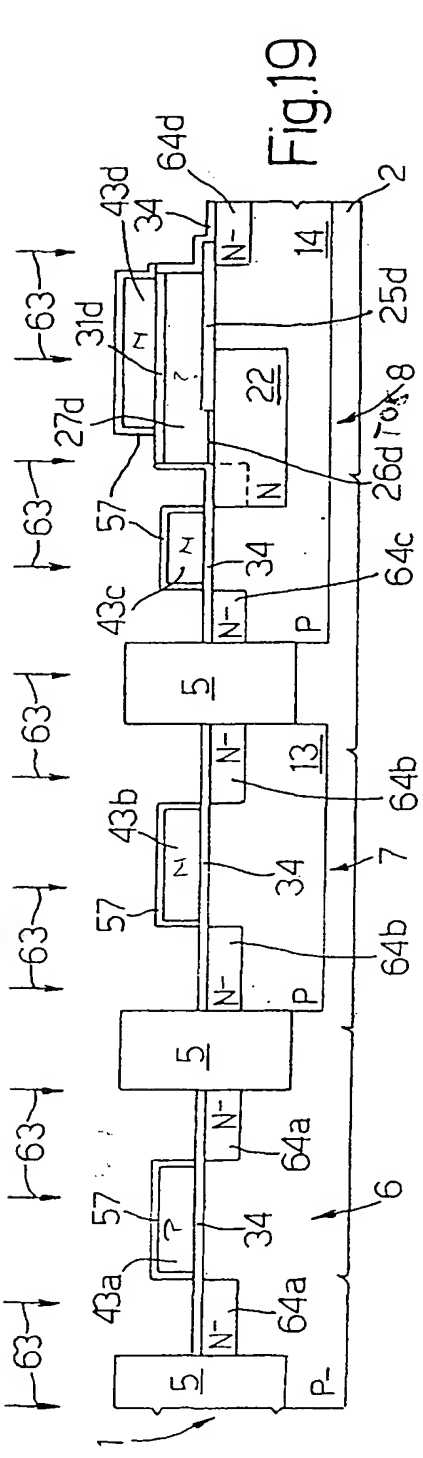
Fig.19
1
2
5
P-
N-
P
N
63
64a
64b
64c
64d
6
7
8
13
14
22
25d
26d
27d
31d
34
43a
43b
43c
43d
57

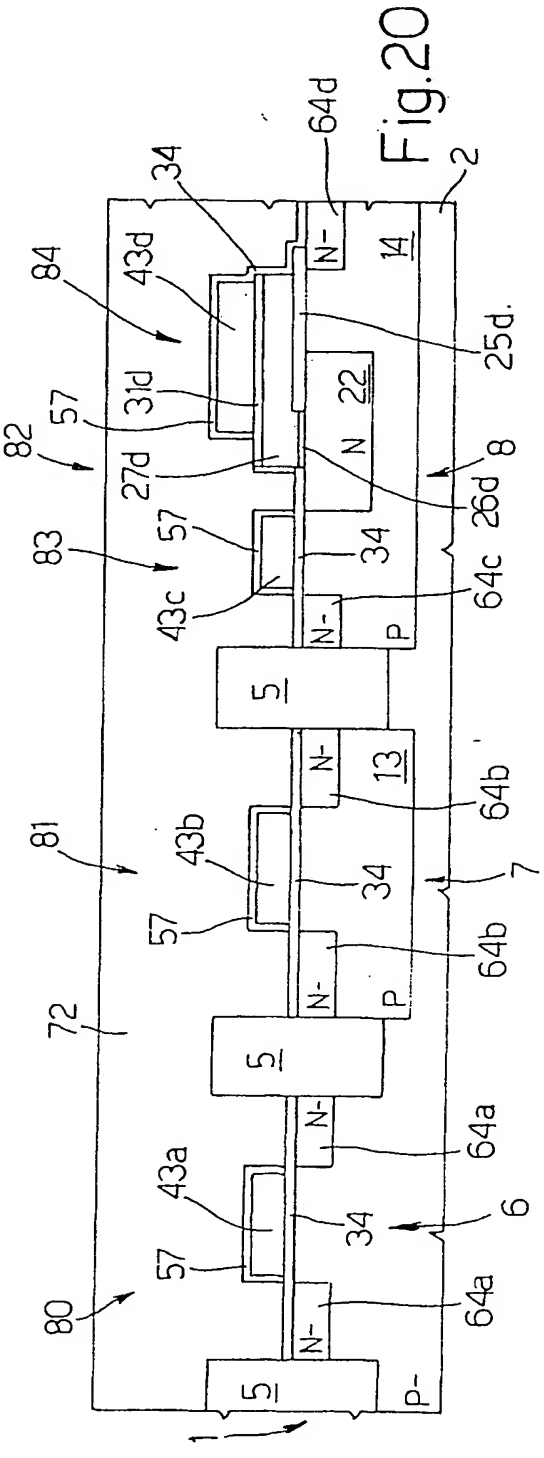
Fig.20
1
2
5
P-
N-
P
N
64a
64b
64c
64d
6
7
8
13
14
22
25d.
26d
27d
31d
34
43a
43b
43c
43d
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EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0717

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Place of search	Date of completion of the search	Examiner
THE HAGUE	18 April 2000	Albrecht, C

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